REMARKS

This paper responds to the Office Action mailed on February 14, 2007.

Claims 1, 7, 8, 13, 21, and 25 are amended. Claims 1-30 remain pending in this application.

§102 Rejection of the Claims

Claims 1-4, 7, 10-14, 17-18, and 21-28 were rejected under 35 USC § 102(e) as being anticipated by Kim et al. (U.S. 7,085,798, hereinafter referred to as Kim).

Applicant respectfully traverses for at least the reasons presented below.

Applicant believes that independent claim 1, as amended, is not anticipated by Kim because Applicant is unable to find in Kim everything recited in claim 1. For example, Applicant is unable to find in Kim the things recited in claim 1 such as, a plurality of selectors, each of the selectors including a multiplexing network to select a pair of input values from among a plurality of input values at input nodes of the multiplexing network, each of the selectors also including a sense amplifier coupled to the multiplexing network to generate at least one input data bit based on the pair of input values, wherein "a value of the input data bit corresponds to one of the input values", and an arithmetic unit including adder input nodes coupled to the sense amplifier to receive the at least one input data bit to perform an arithmetic operation on the at least one input data bit and on at least one additional input data bit of a second number to generate a sum of a first number and a second number, wherein each of the first and second numbers includes multiple bits, wherein "one of the input values at the input nodes of the multiplexing network corresponds to one of the bits of the first number".

The Office Action compares a circuit portion 92 and a circuit portion 94 in FIG. 9 of Kim to the multiplexing network of claim 1. As shown in FIG. 9 of Kim, a plurality of signals or input values at g_i, p_i, and k_i are received at input nodes of circuit portions 92 and 94, where "i" is an index number ranging from, e.g., 0 through 7. Kim teaches in col. 3 lines 30-41 that each of g_i, p_i, and k_i is a is a logical *combination* (e.g., AND, exclusive OR, or NOT) of bits a number A a number B, such as,

$g_i = A_i \odot B_i$ (logical "AND" of bits of a number A and a number B)

p_i, = $A_i \oplus B_i$ B_i (logical "exclusive OR" of bits of number A and number B)

$k_i = A_i\_not \odot B_i\_not$ (logical "AND" of bits of A_i_not and B_i_not)

As taught by Kim, numbers A and B are provided at input nodes of an adder 30 of FIG. 7 of Kim. Adder 30 of FIG. 7 operates to add numbers A and B to provide a sum of number A and B. Circuit portions 92 and 94 in FIG. 9 of Kim are potions of a unit 38 in FIG. 7 in which unit 38 is a part of adder 30. As show in FIG. 7 and FIG. 9 and as discussed above, input values g_i, p_i, and k_i at input nodes of circuit portions 92 and 94 in FIG. 9 of Kim do not correspond to bits of number A or B but correspond to logical combinations of bits of numbers A and B. Applicant is unable to find in Kim a teaching or fair suggestion that instead of g_i, p_i, and k_i (logical combinations of bits of numbers A and B), the bits of number A or B can be provided to the input nodes of circuit portions 92 and 94 (multiplexing network). In contrast, claim 1 recites that "one of the input values at the input nodes of the multiplexing network corresponds to a value of one of the bits of a first number".

The Office Action also compares a sense amplifier in FIG. 9 of Kim to the sense amplifier of claim 1. As shown in FIG. 9 of Kim, the sense amplifier in sum circuit 96-1 is coupled to circuit portions 92 and 94 to generate *sum* S1 and its complementary $S1^-$ based on input values at the input nodes of circuit portions 92 and 94. Thus, even if the bits of number A or B are provided at the input nodes of circuit portions 92 and 94, the sense amplifier in FIG. 9 of Kim is coupled to circuit portions 92 and 94 to generate a *sum* (of *two* bits) based on input values input nodes of circuit portions 92 and 94. In contrast, claim 1 recites a sense amplifier coupled to the multiplexing network to generate at least one input data bit based on the pair of input values, wherein "a value of the input data bit corresponds to one of the input values".

The reasons presented above demonstrate that claim 1 is not anticipated by Kim. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 1. Dependent claims 2-4 depend from claim 1 and recite the things of claim 1. Thus, Applicant believes that claims 2-4 are not anticipated by Kim for at least the reasons presented above regarding claim 1, plus the additional things recited in claims 2-4. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 2-4.

Applicant believes that independent claim 7, as amended, is not anticipated by Kim because Applicant is unable to find in Kim everything recited in claim 7. For example, for at least the reasons presented above regarding claim 1, Applicant is unable to find in Kim the things recited in claim 7 such as, a multiplexing network including a first multiplexer and a second multiplexer, the first multiplexer having first input nodes to receive a plurality of first input values and a first multiplexing output node, the second multiplexer having a second multiplexing output node and second input nodes to receive a plurality of second input values, wherein "each of the second input values is a complementary value of one of the first input values", wherein the multiplexing network passes a selected first input value of the first input values and a selected second input value of the second input values to the first and second multiplexing output nodes when the selected first and second input values are selected by the first and second multiplexers; and a sensor having input nodes coupled to the first and second multiplexing output nodes to receive the selected first and second input values to generate a first input data bit and a second input data bit, wherein "a value of the first input data bit corresponds to one of the first input values, and wherein a value of the second input data bit corresponds to one of the second input values", the sensor also having output nodes to provide the first and second input data bits. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 7. Dependent claims 10-12 depend from claim 7 and recite the things of claim 7. Thus, Applicant believes that claims 10-12 are not anticipated by Kim for at least the reasons presented above regarding claim 7, plus the additional things recited in claims 10-12. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 10-12.

Applicant believes that independent claim 13, as amended, is not anticipated by Kim because Applicant is unable to find in Kim everything recited in claim 13. For example, Applicant is unable to find in Kim the things recited in claim 13 such as "a plurality of first multiplexing networks to receive first input values corresponding to bits of a first number ", "a plurality of first sense amplifiers, each of the first sense amplifiers coupling to one of the first multiplexing networks to generate a pair of input data bits based on the first input values", "a plurality of second multiplexing networks to receive second input values corresponding to bits of a second number", and "a plurality of second sense amplifiers, each of the second sense

amplifiers coupling to one of the second multiplexing networks to generate a pair of input data bits based on the second input values".

The Office Action compares circuit portion 92 and circuit portion 94 in FIG. 9 of Kim to the first and second multiplexing networks of claim 13. However, as shown in FIG. 9 of Kim, circuit portions 92 and 94 (first and second multiplexing networks) of Kim receive the same input values (the same g_i, p_i, and k_i) and not first input values and second input values. In contrast, claim 13 recites a plurality of first multiplexing networks to receive "first input values" corresponding to bits of a first number, and a plurality of second multiplexing networks to receive "second input values". Further, as discussed above regarding claim 1, the input values (g_i, p_i, and k_i) at the input nodes of circuit portions 92 and 94 correspond to logical *combinations* of bits of two numbers A and B and not corresponding to bits of number A or number B. Applicant is unable to find in Kim a teaching or fair suggestion that the input values at the input nodes of circuit portions 92 and 94 can be different (e.g., first input values and second input values) and that the input values at the input nodes of circuit portion 92, or circuit portion 94, or both, can correspond to bits of a first number (e.g., number A) and bits of a second number (e.g., number B). In contrast, claim 13 recites that "a plurality of first multiplexing networks to receive first input values corresponding to bits of a first number" and "a plurality of second multiplexing networks to receive second input values corresponding to bits of a second number". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 13. Dependent claims 14, 17, and 18 depend from claim 13 and recite the things of claim 13. Thus, Applicant believes that claims 14, 17, and 18 are not anticipated by Kim for at least the reasons presented above regarding claim 13, plus the additional things recited in claims 14, 17, and 18. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 14, 17, and 18.

Applicant believes that independent claim 21, as amended, is not anticipated by Kim because Applicant is unable to find in Kim everything recited in claim 21. For example, for at least the reasons presented above regarding claim 1, Applicant is unable to find in Kim the things recited in claim 21 such as, at least one selector to select a pair of input values from among a plurality of input values at input nodes of the multiplexing network, wherein "one of the input values at the input nodes of the multiplexing network corresponds to a value of one of multiple

bits of a first number", the at least one selector including a sense amplifier to generate at least one input data bit based on the pair of input values, wherein "a value of the input data bit corresponds to one of the input values". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 21. Dependent claims 22-24 depend from claim 21 and recite the things of claim 21. Thus, Applicant believes that claims 22-24 are not anticipated by Kim for at least the reasons presented above regarding claim 21, plus the additional things recited in claims 22-24. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 22-24.

Applicant believes that independent claim 25, as amended, is not anticipated by Kim because Applicant is unable to find in Kim everything recited in claim 25. For example, for at least the reasons presented above regarding claim 1, Applicant is unable to find in Kim the things recited in claim 25 such as, at least one selector to select a pair of input values from among a plurality of input values at input nodes of the multiplexing network, wherein "one of the input values corresponds to a value of a bit of multiple bits of a number" and "a value of an input data bit of the pairs of first input data bits corresponds to one of the input values". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 25. Dependent claims 24-28 depend from claim 25 and recite the things of claim 25. Thus, Applicant believes that claims 24-28 are not anticipated by Kim for at least the reasons presented above regarding claim 25, plus the additional things recited in claims 24-28. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 24-28.

Allowable Subject Matter

Claims 5, 6, 8, 9, 15, 16, 19, 20, 29, and 30 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 5, 6, 8, 9, 15, 16, 19, 20, 29, and 30 depend from their respective independent claims 1, 7, 13, 21, and 25. In view of the reasons presented above regarding claims 1, 7, 13, 21, and 25, Applicant believes that claims 5, 6, 8, 9, 15, 16, 19, 20, 29, and 30 are allowable in the depend form. Accordingly, Applicant requests allowance of claims 5, 6, 8, 9, 15, 16, 19, 20, 29, and 30.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 14th day of May 2007.

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